



White Paper

M-WP008

Key Design Considerations for Reliable Flash Storage Products in Industrial & Defense Applications

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Introduction

In recent years, NAND Flash technology has made great strides in terms of memory density, resulting in solid-state drives (SSDs) that now offer multiple terabytes of capacity in highly compact formats. Due to the relative size of the market, component vendors have focused on the requirements of datacenters and consumers as well as usage profiles. Although component vendors focus on the needs of consumers and data centers, the leading edge component technologies can be leveraged into designs targeting industrial applications.

Industrial users have stringent requirements for resilience, fault tolerance and sustained operation in extreme environments. NAND Flash memory-based SSD technology can remain accessible if the products they use are implemented with a focus on these needs. The key is to couple careful characterization of memory devices and controllers with product design that accounts for industrial use-cases.



Remaining reliable in harsh environments

A major factor in the reliability and resilience of Flash that is of concern to industrial users is its performance under changes in temperature. All NAND Flash memory technologies in use today exhibit changes in behavior with temperature, particularly in the case of data retention. Flash memory technology is based on the principle of a floating gate transistor. To program or erase a Flash memory cell, charge carriers are injected into or removed from the floating gate to alter the threshold voltage of the floating gate transistor to different levels (or states) to distinguish stored data values. The length of time that a Flash memory cell can retain the original programmed state is shortened as the temperature increases.

There are significant differences among types of NAND Flash memories. This is due to the many design and manufacturing tradeoffs the component vendors make. Single-level cell (SLC) NAND technology provide superior retention time under a wider range of conditions than those typically encountered in the consumer space, but with a significant cost premium and density limitation. Multi-level cell (MLC), triple-level cell (TLC) and quadruple-level cell (QLC) NANDs offer high densities and progressively better cost per bit advantage at the expense of data reliability. The migration of NAND memory architecture from 2D to 3D with the shift from traditional poly-silicon to a charge-trapping floating gate presents another dimension in the challenge to choose the right NAND components to build SSD products for industrial applications.

One choice the SSD designer can make when using high-density NAND is to opt for pseudo single-layer cell (pSLC) operation for critical data files and objects. This mode stores single bits in cells that are normally employed for multiple bits, delivering tenfold greater write endurance that improves overall error-free lifetime.

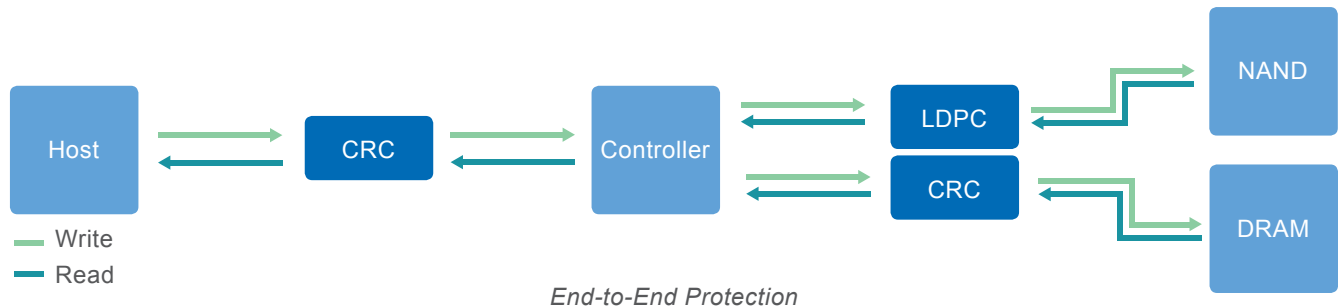
SLC	1				0			
pSLC	111	110	101	100	000	010	001	011
3D TLC	111	110	101	100	000	010	001	011

Structure of Data Storage in NAND

SMART Modular Technologies (SMART) has established its own in-house NAND Flash characterization capability to identify suitable NAND components, validate their specifications and establish the safe operating limits of each beyond core specification. From these, SMART chooses the most suitable NAND components for SSD products appropriate for the market segments and applications.

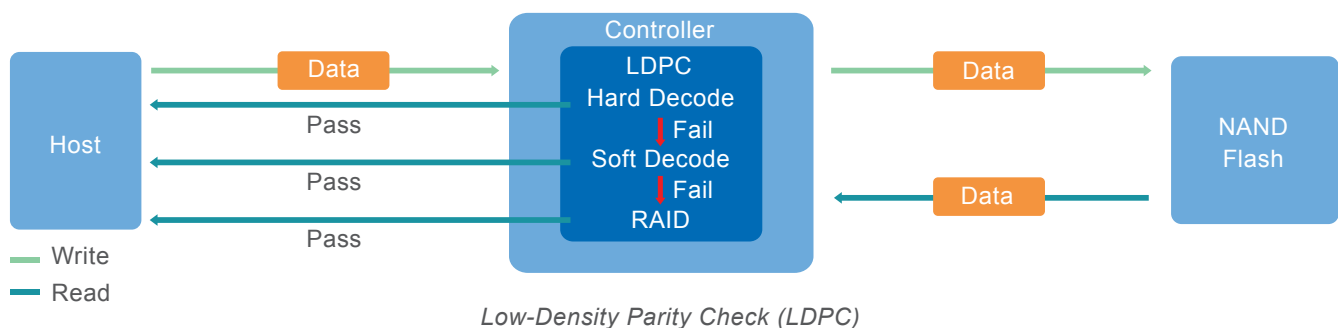
SSD design considerations

The same characterization and selection process applies to the controllers that are used to manage the Flash memory in the SSDs. An emphasis on architectures that can ensure end-to-end protection along the data path is placed from the host interface through to the Flash storage media. In addition, many controllers cache data in volatile SRAM or DRAM buffer before writing it to non-volatile Flash to improve performance. In more resilient designs, the volatile memories and buses used to transfer data are protected by cyclic redundancy check (CRC) and error correction code (ECC) hardware and firmware algorithms to ensure no bits are corrupted at any point along this path. This protection is especially important for airborne because of possibility of radiation-induced bit flips. In addition, SMART designs and tests its products to withstand the low atmospheric pressure up to 80,000 ft.

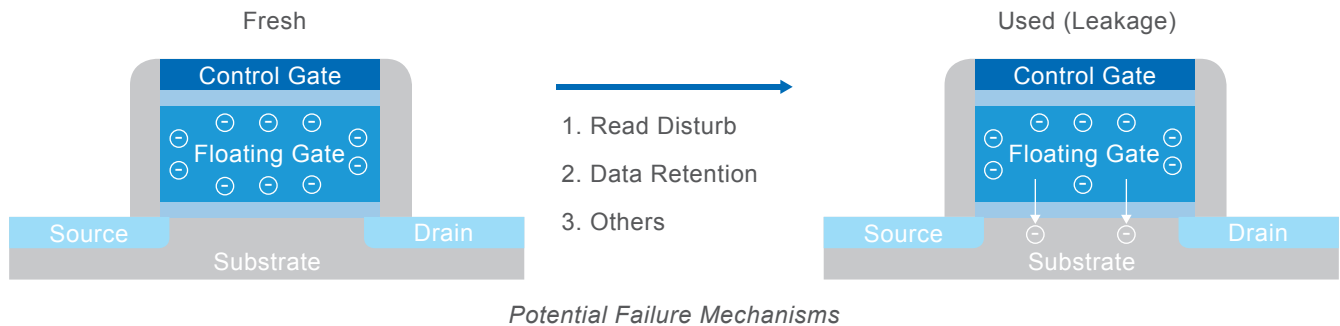


ECC is utilized to detect and correct stored data in Flash memory forms is a key factor in the selection process for controllers in industrial SSD designs. ECC with the right amount of error correction strength provides a method to limit the impact of errors from data retention degradation over time at elevated temperatures. Conventional ECC, such as Hamming, Reed-Solomon and Bose-Chaudhuri-Hochquenghem (BCH) codes, have been the proven workhorse in 2D NAND SSD controllers for more than two decades. With the advent of TLC and QLC 3D NAND technology, the error conditions that SSD controller designers face are more complex. Originally applied to noisy wireless communications channels such as those encountered in space exploration, low-density parity check (LDPC) provides far greater resilience to the errors encountered in 3D NAND Flash and is favored on new SSD controller designs.

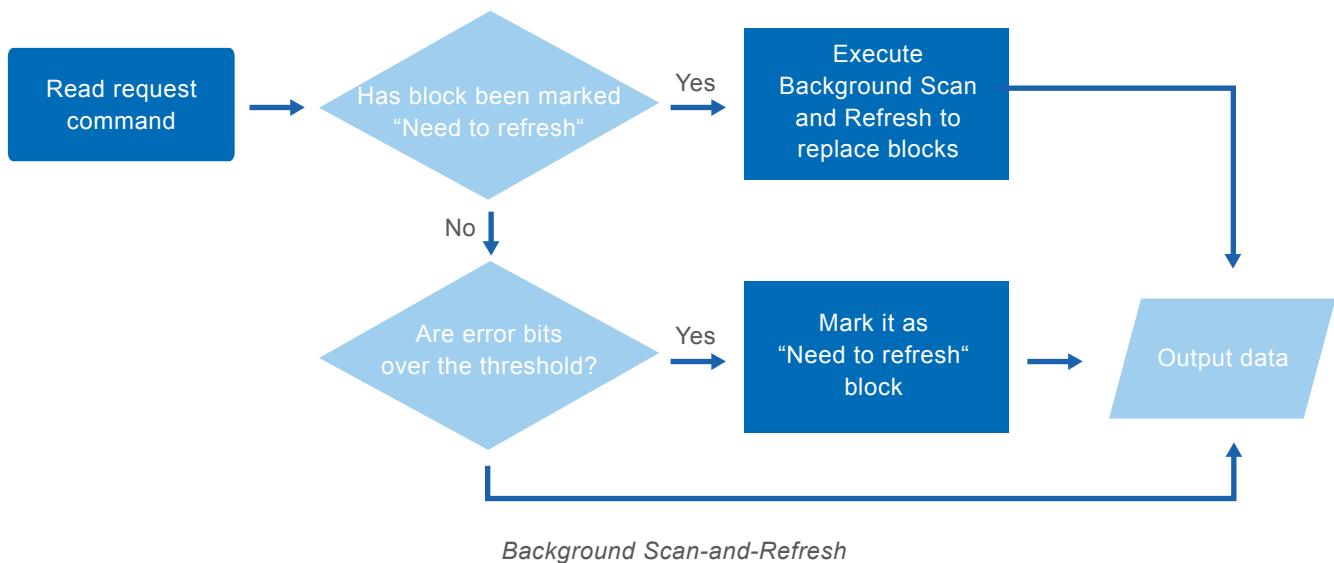
The main benefit of LDPC codes lies in its high error correction strength with the least amount of data storage overhead. LDPC can also utilize “soft” data in addition to the raw “hard” data as read from Flash memory in its iterative decoding algorithm, which reconstructs data from noisy sources. However, not all LDPC implementations in SSD controllers are the same. When designing industrial-grade SSDs with 3D NAND, SMART engineers first establish the raw error rates of suitable Flash devices using both the manufacturer specifications and the results of their own characterization results. They then choose the most appropriate SSD controller: one that employs an LDPC engine that has sufficient error-correction strength and code efficiency to ensure overall data integrity and reliability, while providing the expected performance of the SSD.



Though ECC provides a high degree of protection, the reliability and resilience of Flash-based SSDs can be improved further by taking account of other potential failure mechanisms. The incredibly fine geometries and dense packing of the Flash memory cells lead to interference in neighboring cells when data elements are accessed. This interference leads to the phenomenon called “read disturb” where reading data located on one word line repeatedly can cause changes to data on adjacent word lines over time. Robust industrial-grade SSDs, such as those supplied by SMART, employ firmware algorithms to monitor the number of reads and refresh the data before the data errors introduced by the state changes induced in the memory cells reach a critical level.



The same care goes into the design of the controller’s garbage-collection and wear-levelling algorithms which go into how efficient the physical Flash memory is utilized in operation. These algorithms avoid incurring excessive wear to any part of the storage array by optimizing the data movement to lesson and even out the wear of the physical memory. Industrial-grade controllers take one step further by automatically scanning stored data in the background periodically based on criteria such as device on and idle time, wear of the physical memory, operating temperature, etc. Data that are identified to have higher than average error rates by the ECC circuitry are rewritten, i.e. refreshed, where needed. The automatic background scan-and-refresh is a key technique SMART utilizes to offset the effect of data retention loss at elevated temperature.



Additional considerations

Application design also plays a part in Flash-based SSD reliability. A single drive may be used for several different types of data, from infrequently accessed large files through important, frequently read configuration data to very small files used for checkpointing purposes that are written many times a day. These file types need not be stored the same way. Giving the host computer some control over their storage makes it possible to improve overall service life and reliability.

The impact of different write behaviors can be more subtle, leading to differences in the write amplification factor (WAF). This is a metric that determines the amount of data that needs to be written and rewritten on the drive in response to the data transferred to the SSD's host interface. For example, each small file that is written will at first be assigned to its own page. To improve utilization, the drive may consolidate those small files onto one page, which increases the overall number of writes. Though it may be necessary to use small file updates to ensure systems hold an accurate reflection of their state due to power or other interruptions, systems can organize writes to match the page size as best they can through a combination of smarter firmware that consolidates blocks before writing them and through application architecture. For example, datalogging software can ensure it performs writes that are matched to the target SSD's page size.

SMART's industrial-grade SSDs provides extended Self-Monitoring, Analysis, and Reporting Technology (S.M.A.R.T.) health monitoring data reporting for the host system monitor the health of the SSDs when in use.

In addition to the care in choosing the right components and controllers for specific SSD products, SMART uses burn-in and test procedures in manufacturing to make sure drives with a higher probability of early failure do not enter the supply chain.

By choosing products that are characterized and tested for the industrial environment, systems builders and manufacturers can take advantage of the explosion in non-volatile storage capacity made possible by Flash memory. The experience that SMART offers in this area will be invaluable to developers of industrial control and computing systems.



For more information, please visit: www.smartm.com

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